REMARKS

Applicants have carefully reviewed the Office Action dated July 26, 2005. Applicants have amended Claims 1, 2, 5, 6, 9, 10, 13 and 14 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

The drawings have been objected to as the Examiner considers that they fail to show the "gain controller" in Claim 9. Claim 9 has been amended to refer to a "gain control input" as opposed to a "gain controller." As such, Applicants do not believe that the drawings are required to be amended. Further, formal drawings were filed on August 16, 2005.

Claims 1-16 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. This rejection is respectfully traversed with respect to the amended claims.

The Examiner has noted that, with respect to Claim 1, the recitation "a first rate" and "a second rate" are inconsistent. Applicants believe that the Examiner is confused as to what the term "rate" refers to. This clearly refers to the clock rate. It can be seen that charge is dumped onto the sampling node (120) with the switch (118) under control of the signal φ_2, whereas the charge on the capacitor C2 is dumped onto the sampling node 120 with the switch 156 under the control of the AND function of clock signal φ_2 and φ_A. As such, it can be seen from the timing signals of Fig. 2 that the clock rate of the two is different. Thus, by controlling the clock rate of φ_A, the amount of charge dumped onto the node 120 can be changed and, thus, the gain can be changed. Thus, the term "rate" clearly refers to the clock rate. The claims have been amended accordingly and, as such, Applicants believe that this overcomes the rejection with respect to Claim 1 under 35 U.S.C. §112.

The Examiner has also indicated that the term "substantially the first rate" is indefinite because it is mis-

descriptive. Applicants believe that this is not the case. The reason for this is that, with any integrated circuit, even though a clock signal is generated at a first rate, there can be jitter associated with the circuitry associated with driving that clock signal to the switch. As such, the actual clock rate may change, although the average clock rate is "substantially" the clock rate of the first clock rate. Therefore, there will be subtle differences between the two clock rates. This is an inherent aspect of any integrated circuit due to the propagation path for propagating a clock from a clock generation circuit to any portion of an integrated circuit. Therefore, Applicants believe that the use of the term "substantially" is correct, as interpreting the clock rate to be "exact" is not consistent with the generally known operation of an integrated circuit and the generation and propagation of clocks throughout. As such, Applicants believe that this recitation is correct.

With respect to Claim 2, the Examiner has objected to the language "in phase from the first clock and synchronous therewith." This language basically refers to the fact that these clocks are synchronous and that all edges of the clocks are referenced to some common timing source. Applicants have not stated that the clocks are equal in phase but, rather, the term "in phase" is indicated as being associated with the term "shifted in phase." All this means is that there is a phase difference between the two clocks. If they were in phase, both rising edges would occur at substantially the same time and both falling edges would also occur at substantially the same time. In the specification, paragraph [0012], line 2, (on page 8), it is set forth that these two signals are non-overlapping clocks. Non-overlapping clocks are generally considered, with respect to switched-capacitor operation, to be synchronous to the same timing source. Further, the claims clearly state that these are synchronous and, if there is any confusion that this is not supported in the specification, the claims, since they were originally filed, can be utilized for this support. In any event, it is common to refer to non-overlapping clocks used with a switched-capacitor circuit as synchronous. If anything other were assumed, the circuit could not work. As such, Applicants believe that the language of Claim 2 is clear.

With respect to Claim 9, the use of the term "a first rate" and a "second rate" is believed to be corrected with the inclusion of the term "clock" therein. The use of the term "substantially at the first rate" has been addressed with respect to Claim 2. The use of the term "a second time" was not addressed herein above, but it clearly refers to the fact that the signal φ_2 is substantially 180° that of phase with the clock signal φ_1.

Therefore, charge is sampled onto the sample capacitor at one time and then transferred therefrom to the sampling point at a second time. This is clearly described in the specification with respect to the timing diagram. The Examiner has also indicated that there was some problem with the recitation "sampling the input voltage onto the feedback sampling capacitor" on line 7 thereof. However, line 7 states that "a first dump circuit for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier at a second time and at the first rate; . . .". Clearly, this refers to switch (118), which clearly dumps charge from the input sampling capacitor to the non-inverting input of the amplifier at the second time. As such, Applicants do not understand which portion of the claim the Examiner is referring to. Claim 9 refers to sampling "a reference voltage" onto a feedback sampling capacitor and this is believed to be correct. Applicants request that the Examiner provide clarification for this comment in the *Office Action*. As to the term "gain controller," this has been changed. As to controlling the "amount of time" a charge is dumped from said feedback sampling capacitor to be substantially equal to the amount of time that charge is being dumped from the input sampling capacitor, this is merely the way of changing the clock rate. Whatever a clock rate of φ_A is, this will determine the gain. This has been corrected to set forth that the control signal basically controls the amount of time that a charge is dumped from the feedback sampling capacitor "relative to" the amount of time that charge is being dumped from the input sampling capacitor.

With respect to Claim 10, these issues have been addressed with respect to the discussion of Claim 2 herein above.

In view of the above, Applicants believe that the claims have now been amended or clarified to overcome the 35 U.S.C. §112 rejection with respect to and, therefore, the withdrawal of the 35 U.S.C. §112 rejection with respect to Claims 1-10 is respectfully requested.

Claims 1-16 stand rejected under 35 U.S.C. §102(b) as being anticipated by *Shin*. This objection is respectfully traversed with respect to the amended claims.

The Examiner has specifically referred to Figs. 6 and 7 of *Shin* for disclosing a method for driving the

input of an integrator. However, Applicants believe that with the clarifications herein above, that *Shin* is not relevant. *Shin* provides gain control, but the gain control is provided by the feedback resistor and capacitor combination (3). All that the input switch capacitor devices provide is to provide a conversion from a differential input to a single-ended input. It can be seen that there is no different clock rate for transferring charge to the negative input terminal of the amplifier (4). The specification clearly states that these clocks all operate at the same rate and that there is no ability to change the rates for transferring charge. As such, Applicants believe that the *Shin* reference does not anticipate or obviate Applicants' inventive concept, as defined by the amended claims. Therefore, Applicants respectfully request the withdrawal of the 35 U.S.C. §102(b) rejection with respect to Claims 1-16.

Applicants have now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicants respectfully request full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/CYGL-26,655 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
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January 19, 2006

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